IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Manpreet S. Khaira et al.	Examiner: Samarina Makhdoom	
Serial No.:	09/347,690	Group Art Unit: 2123	
Filed:	July 2, 1999	Docket: 884.107US1	
Title:	LOGIC VERIFICATION IN LARGE SYSTEMS		

RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

The Applicants' representative has reviewed the Office Action mailed on August 27, 2002. Please consider the appended remarks.

REMARKS

The Applicants' representative has carefully reviewed and considered the Office Action mailed on August 27, 2002, and the references cited therewith. No claims are amended, no claims are canceled, and no claims are added. As a result, claims 1-28 are now pending in this Application. Please note that three Affidavits submitted under § 1.131 (from inventors Casas, Seligman, and Yang) are attached hereto as Exhibit A.

Drawings

The Applicants are required to submit a proposed drawing correction in reply to the instant Office Action. The Applicants respectfully decline to comply with this requirement.

It is asserted in the Office Action that Figures 1, 3, and 9 should be labeled as "Prior Art" in consideration of the reference authored by Casas, et al. "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding of VLSI Design, Jan. 7-10, 1999 (hereinafter "Casas"). However, in accordance with the affidavits submitted herewith under § 1.131, Casas is not prior art, and should not be considered as much. Thus, the requirement in the Office Action with respect to Figures 1, 3, and 9 is moot. If the Examiner does not agree with this assessment, in light of the attached affidavits, the Examiner is respectfully requested to contact the Applicants' representative, or the undersigned, at the earliest convenient time in order to rectify the Examiner's concerns.